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**PHASE CONTROL THYRISTOR****AT804**

Repetitive voltage up to **1600 V**  
Mean on-state current **985 A**  
Surge current **12.5 kA**

**FINAL SPECIFICATION**

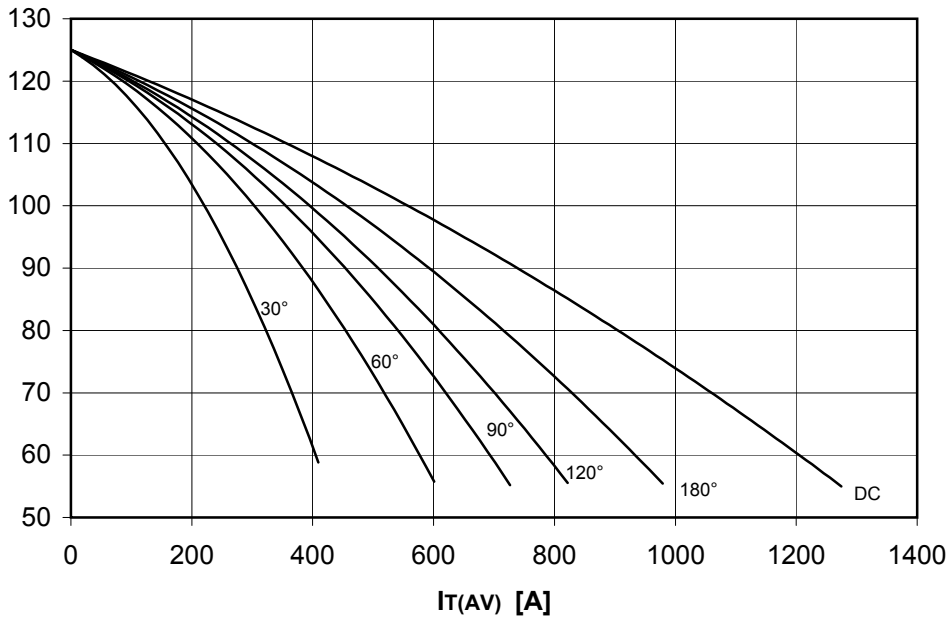
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Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	1600	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	1700	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	1600	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=V <sub>RRM</sub>	125	50	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=V <sub>DRM</sub>	125	50	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		985	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		770	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	125	12,5	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		781 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1600 A	25	1,63	V
V <sub>T(TO)</sub>	Threshold voltage		125	1,0	V
r <sub>T</sub>	On-state slope resistance		125	0,380	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% V <sub>DRM</sub> up to 1050 A, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V <sub>DRM</sub>	125	500	V/μs
td	Gate controlled delay time, typical	VD=100V, gate source 25V, 10 ohm, tr=.5 μs	25	1,1	μs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V <sub>DRM</sub>		200	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt=-20 A/μs, I= 700 A	125		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 50 V			A
I <sub>H</sub>	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	VD=5V, tp=30μs	25	700	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	VD=5V	25	3,5	V
I <sub>GT</sub>	Gate trigger current	VD=5V	25	250	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	VD=V <sub>DRM</sub>	125	0,25	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		37	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		7	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C
F	Mounting force			11.8 / 13,2	kN
	Mass			300	g
<b>ORDERING INFORMATION : AT804 S 16</b>					
standard specification <input type="checkbox"/> <input type="checkbox"/> VDRM&VRRM/100					

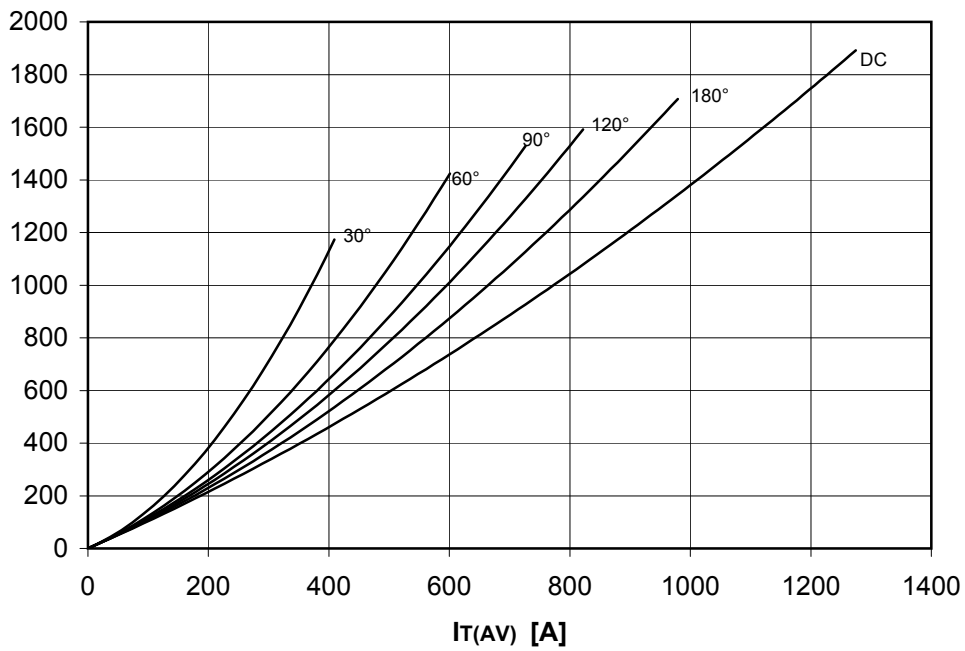
## DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



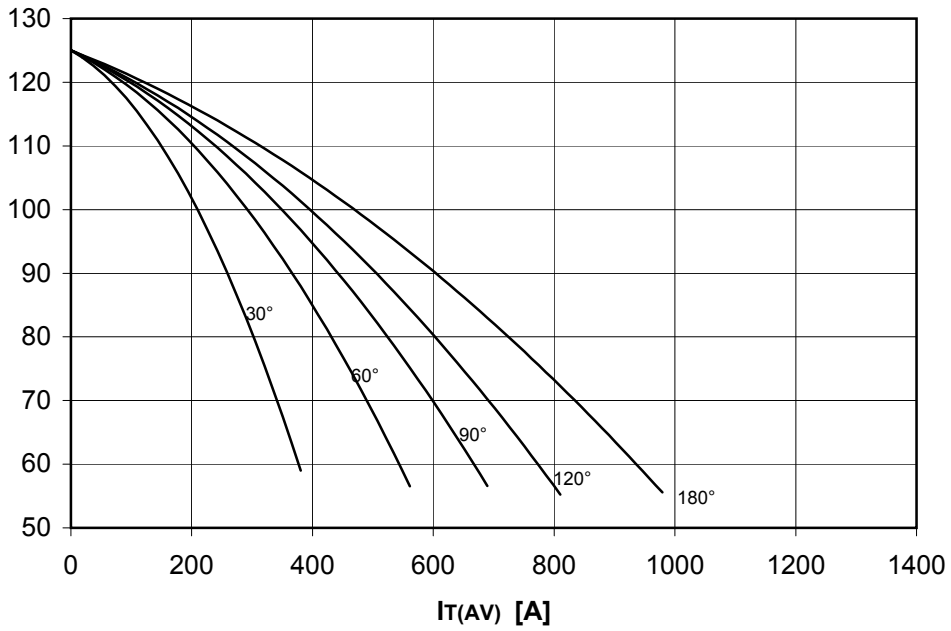
PT(AV) [W]



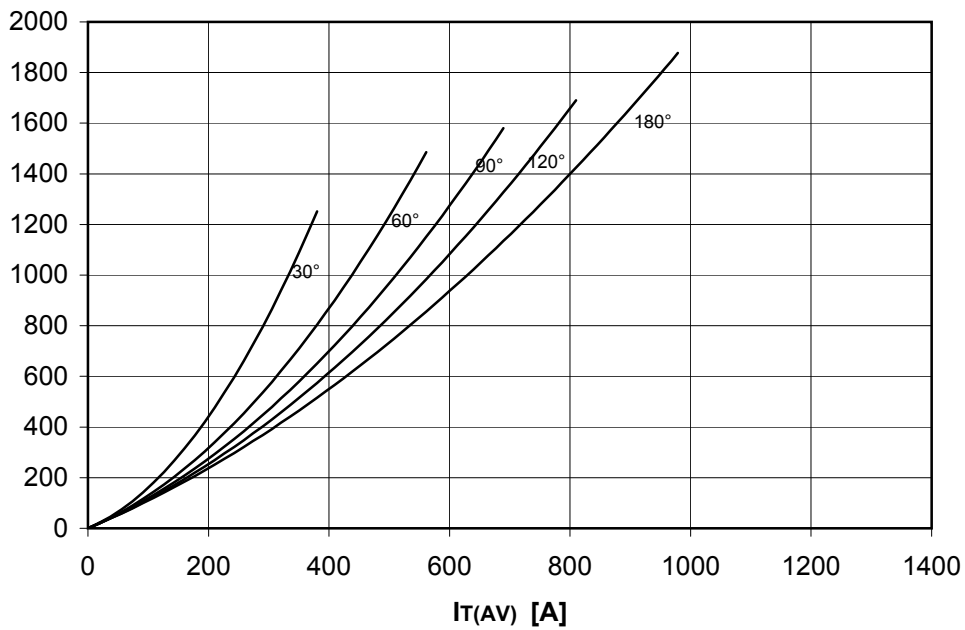
## DISSIPATION CHARACTERISTICS

SINE WAVE

$T_h$  [°C]



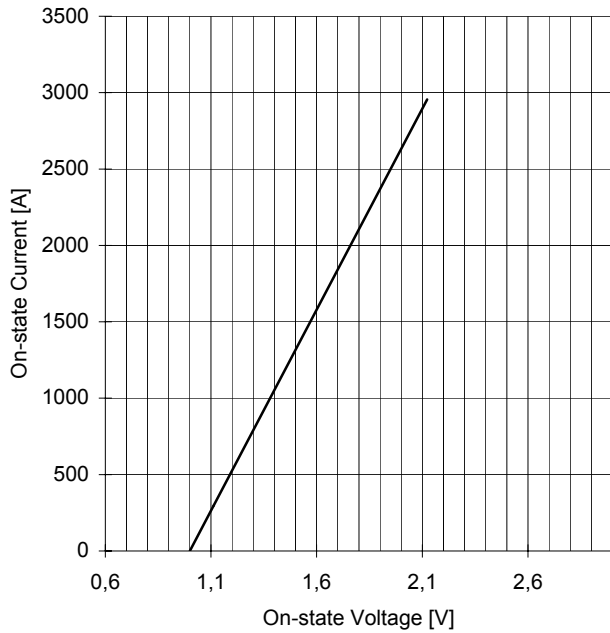
$P_T(AV)$  [W]



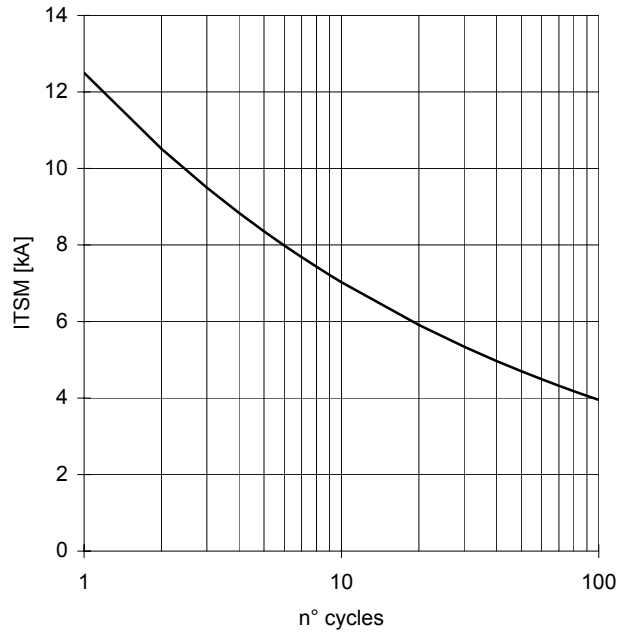
# AT804 PHASE CONTROL THYRISTOR

FINAL SPECIFICATION mag 06 - ISSUE : 05

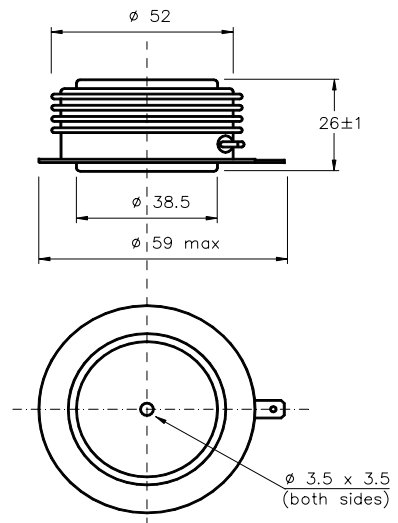
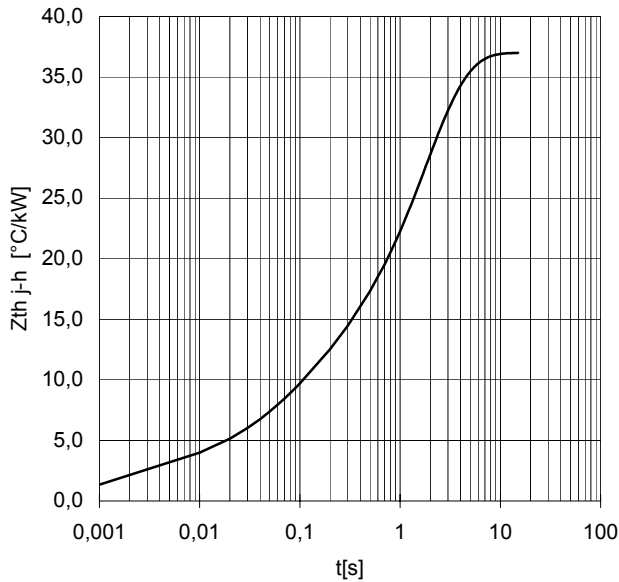
ON-STATE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



SURGE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



Dimensions  
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2  $\mu\text{m}$ .  
In the interest of product improvement POSEICO reserves the right to change any data given in this data sheet at any time without previous notice.  
If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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